FIG. 1

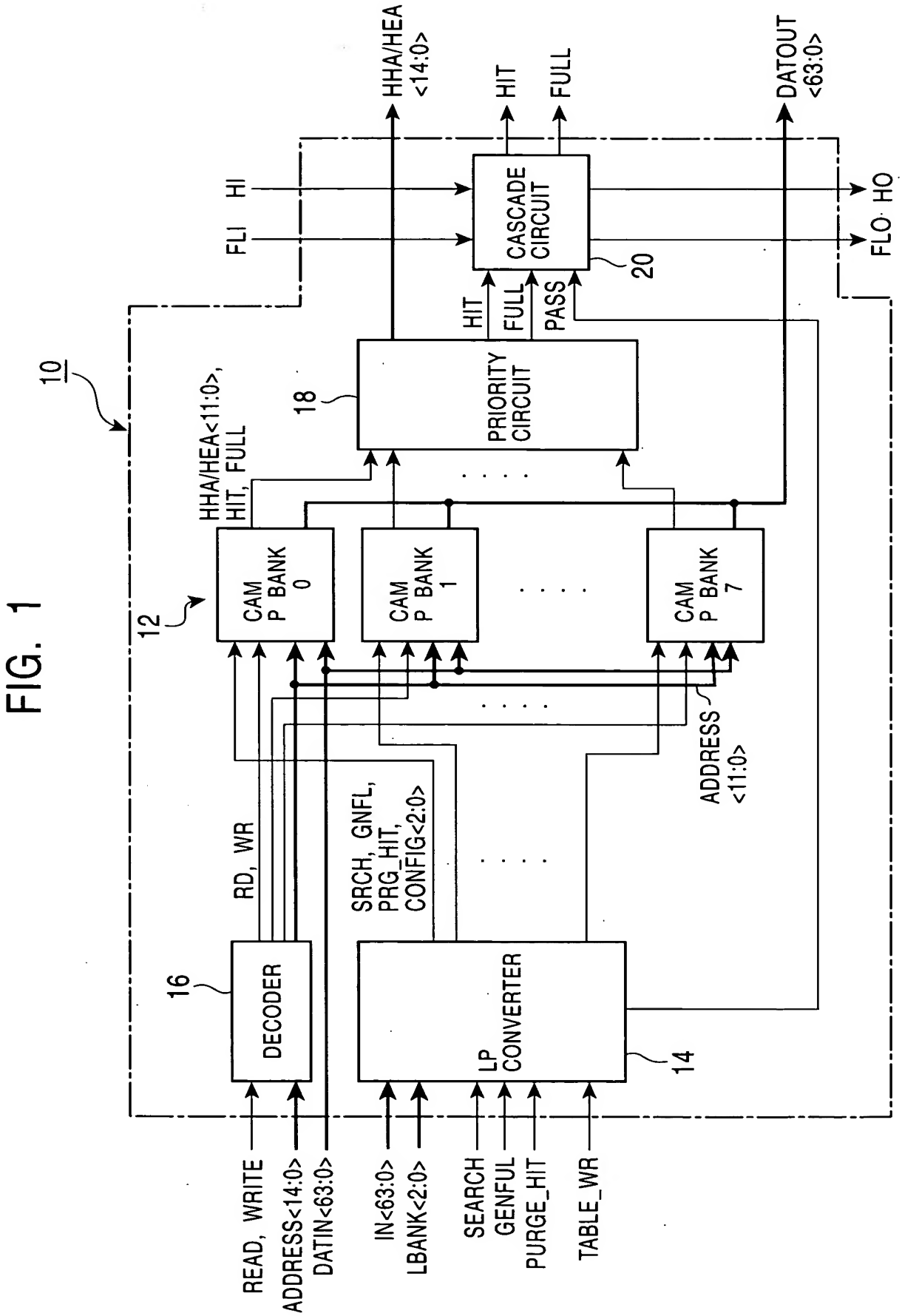

10
12
16
18
20
14
CAM P BANK 0
CAM P BANK 1
CAM P BANK 7
DECODER
PRIORITY CIRCUIT
CASCADE CIRCUIT
LP CONVERTER
HHA/HEA <14:0>
HIT
FULL
DATOUT <63:0>
HI
FLI
FLO
HO
HIT
FULL
PASS
HHA/HEA<11:0>, HIT, FULL
RD, WR
SRCH, GNFL, PRG_HIT, CONFIG<2:0>
ADDRESS <11:0>
READ, WRITE
ADDRESS<14:0>
DATIN<63:0>
IN<63:0>
LBANK<2:0>
SEARCH
GENFUL
PURGE_HIT
TABLE_WR

FIG. 2

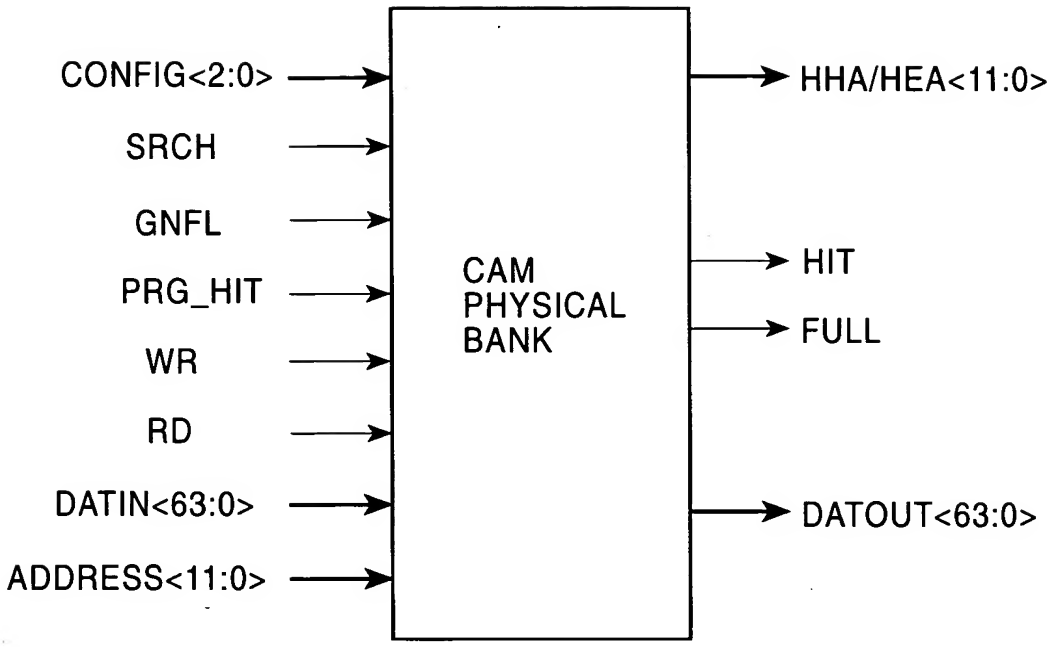

CONFIG<2:0>
SRCH
GNFL
PRG_HIT
WR
RD
DATIN<63:0>
ADDRESS<11:0>
CAM
PHYSICAL
BANK
HHA/HEA<11:0>
HIT
FULL
DATOUT<63:0>

FIG. 3A

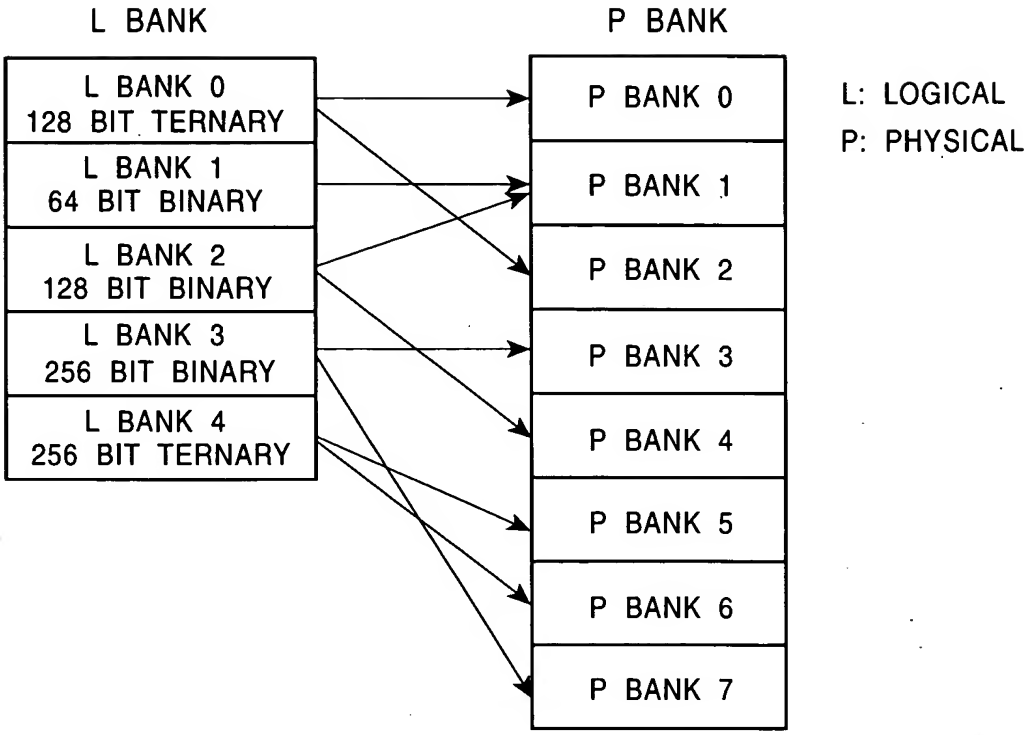


FIG. 3B

L BANK	CONFIG<2:0>
64 BIT BINARY	000
128 BIT BINARY	001
256 BIT BINARY	010
64 BIT TERNARY	100
128 BIT TERNARY	101
256 BIT TERNARY	110

FIG. 4

	P BANK 0	P BANK 1	P BANK 2	P BANK 3	P BANK 4	P BANK 5	P BANK 6	P BANK 7	TABLE CONFIGU-RATION	TABLE OUTPUT	CONFIG <2:0>
L BANK 0	1	0	1	0	0	0	0	0	128 BIT TERNARY	10100000	101
L BANK 1	0	1	0	0	0	0	0	0	64 BIT BINARY	01000000	000
L BANK 2	0	1	0	0	1	0	0	0	128 BIT BINARY	01001000	001
L BANK 3	0	0	0	1	0	0	0	1	256 BIT BINARY	00010001	010
L BANK 4	0	0	0	0	0	1	1	0	256 BIT TERNARY	00000110	110
L BANK 5	0	0	0	0	0	0	0	0	NOT USED	00000000	
L BANK 6	0	0	0	0	0	0	0	0	NOT USED	00000000	
L BANK 7	0	0	0	0	0	0	0	0	NOT USED	00000000	

ASSIGN = "1"
NO ASSIGN = "0"

FIG. 5

	P BANK 0	P BANK 1	P BANK 2	P BANK 3	P BANK 4	P BANK 5	P BANK 6	P BANK 7
L BANK 0	BIT <0>	BIT <1>	BIT <2>	BIT <3>	BIT <4>	BIT <5>	BIT <6>	BIT <7>
L BANK 1	BIT <8>	BIT <9>	BIT <10>	BIT <11>	BIT <12>	BIT <13>	BIT <14>	BIT <15>
L BANK 2	BIT <16>	BIT <17>	BIT <18>	BIT <19>	BIT <20>	BIT <21>	BIT <22>	BIT <23>
L BANK 3	BIT <24>	BIT <25>	BIT <26>	BIT <27>	BIT <28>	BIT <29>	BIT <30>	BIT <31>
L BANK 4	BIT <32>	BIT <33>	BIT <34>	BIT <35>	BIT <36>	BIT <37>	BIT <38>	BIT <39>
L BANK 5	BIT <40>	BIT <41>	BIT <42>	BIT <43>	BIT <44>	BIT <45>	BIT <46>	BIT <47>
L BANK 6	BIT <48>	BIT <49>	BIT <50>	BIT <51>	BIT <52>	BIT <53>	BIT <54>	BIT <55>
L BANK 7	BIT <56>	BIT <57>	BIT <58>	BIT <59>	BIT <60>	BIT <61>	BIT <62>	BIT <63>

FIG. 6

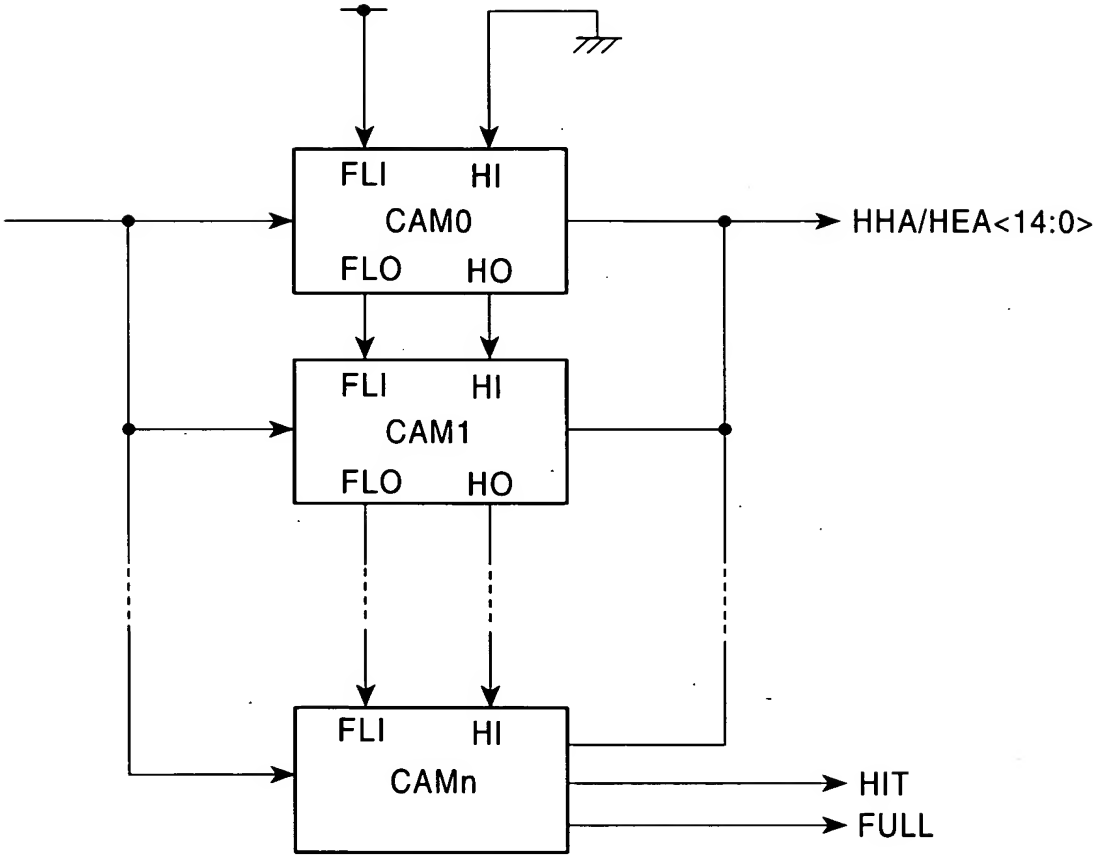
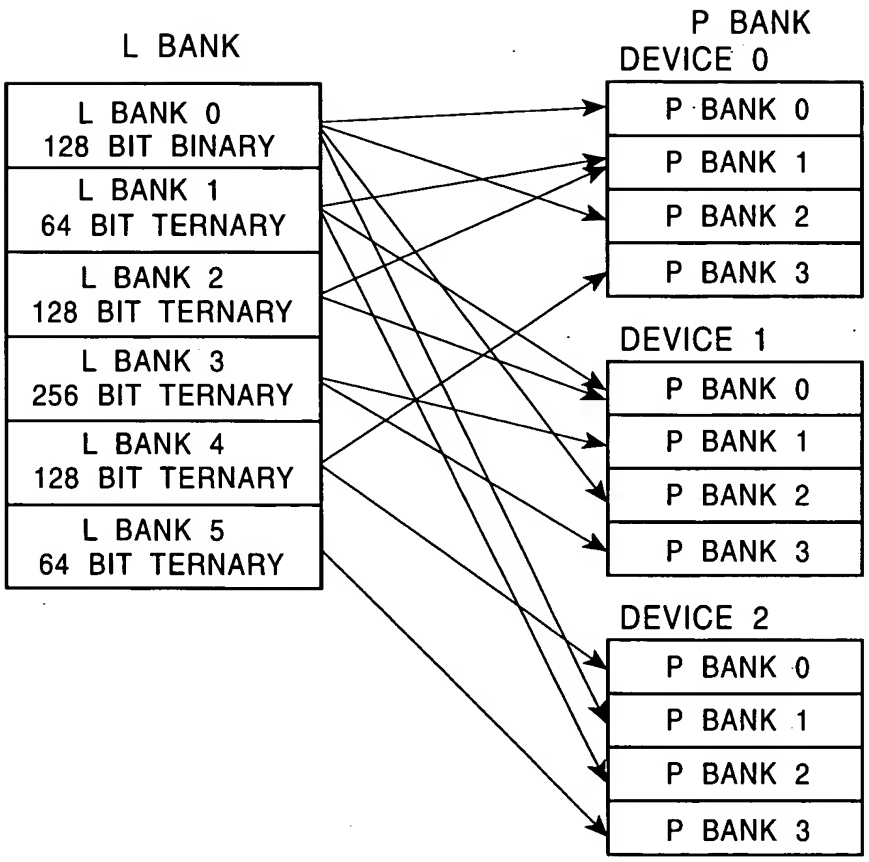

FLI
HI
CAM0
FLO
HO
HHA/HEA<14:0>
FLI
HI
CAM1
FLO
HO
FLI
HI
CAMn
HIT
FULL

FIG. 7


L BANK
L BANK 0
128 BIT BINARY
L BANK 1
64 BIT TERNARY
L BANK 2
128 BIT TERNARY
L BANK 3
256 BIT TERNARY
L BANK 4
128 BIT TERNARY
L BANK 5
64 BIT TERNARY
P BANK
DEVICE 0
P BANK 0
P BANK 1
P BANK 2
P BANK 3
DEVICE 1
P BANK 0
P BANK 1
P BANK 2
P BANK 3
DEVICE 2
P BANK 0
P BANK 1
P BANK 2
P BANK 3

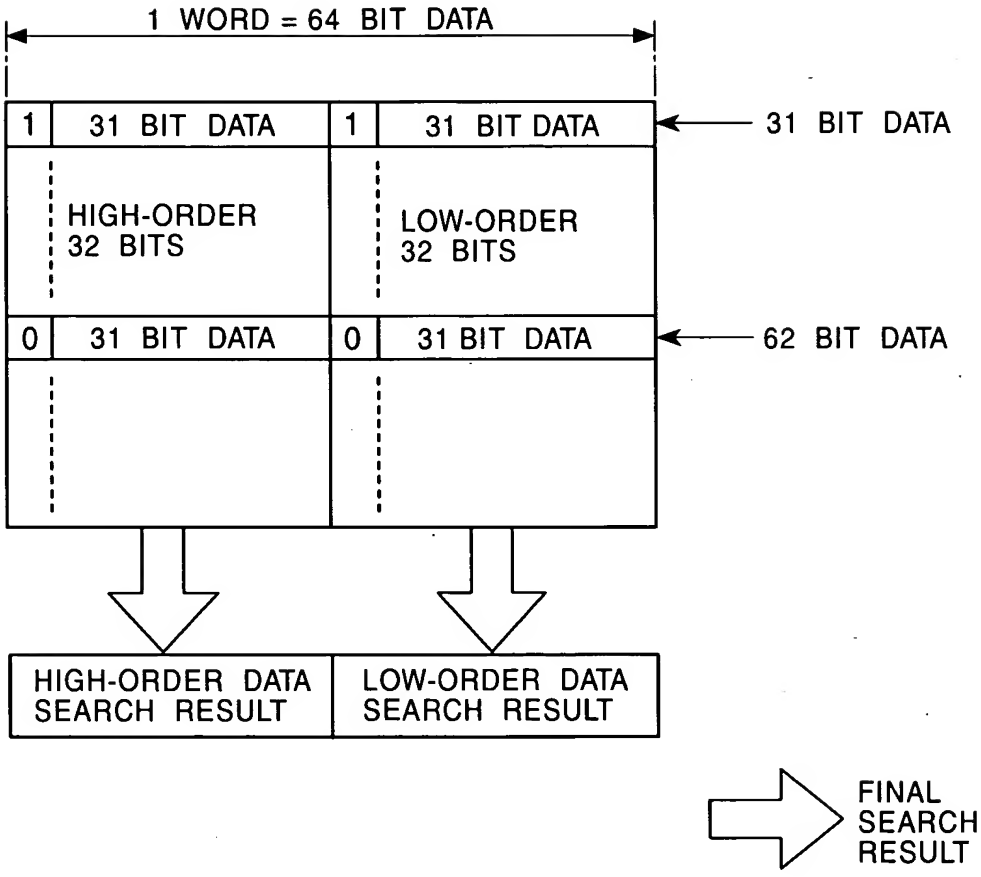



FIG. 8
PRIOR ART